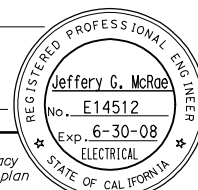


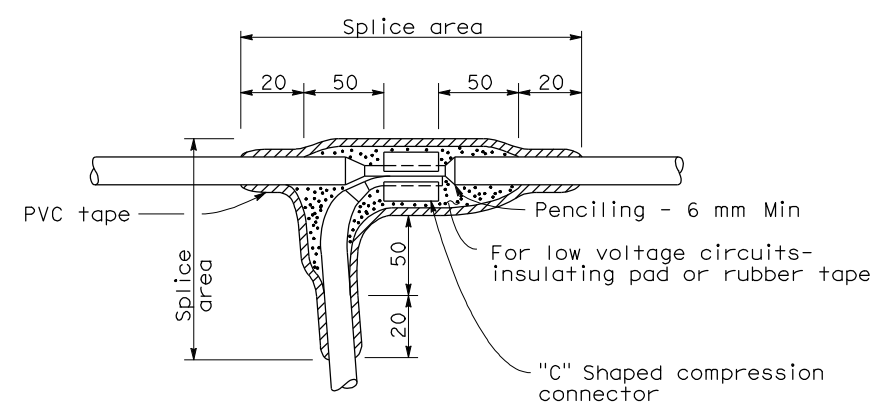


DIST	COUNTY	ROUTE	KILOMETER TOTAL PROJECT	POST TOTAL PROJECT	SHEET NO.	TOTAL SHEETS

REGISTERED ELECTRICAL ENGINEER
Jeffery G. McRae
 REGISTERED ELECTRICAL ENGINEER
 October 5, 2007
 PLANS APPROVAL DATE
 The State of California or its officers or agents shall not be responsible for the accuracy or completeness of electronic copies of this plan sheet.
 To get to the Caltrans web site, go to: <http://www.dot.ca.gov>

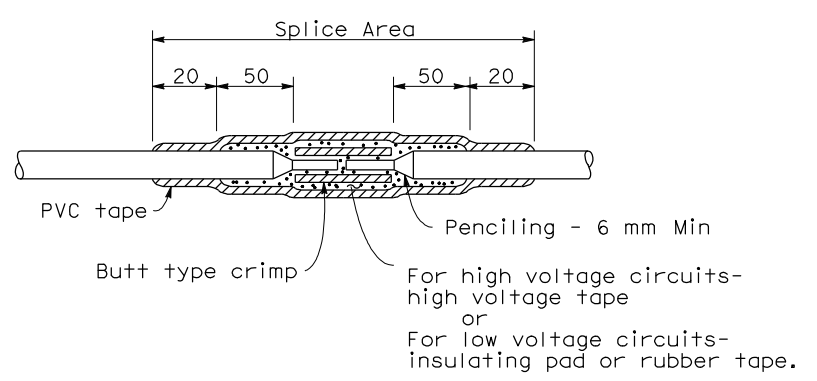


To accompany plans dated _____



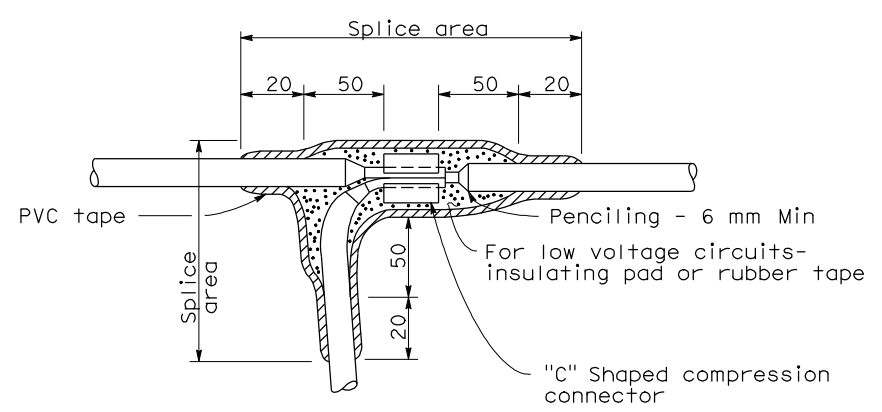
TYPE "C" SPLICE

Between 1 free-end and 1 through conductor



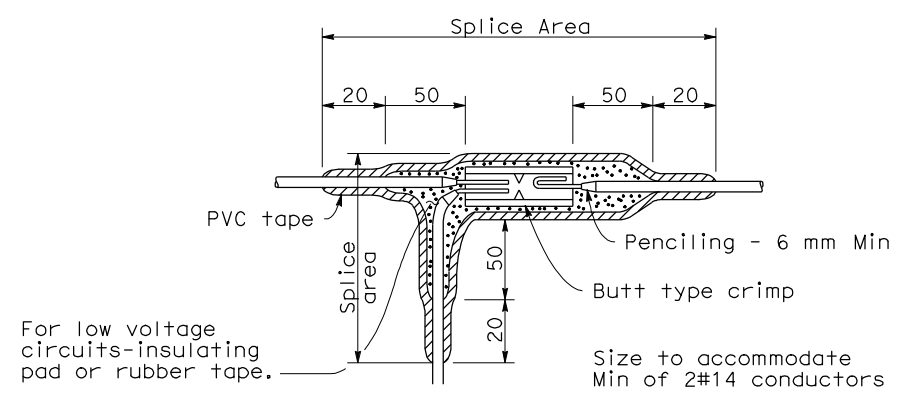
TYPE "S" SPLICE

Between 2 free-ends



TYPE "T" SPLICE

For 3 free-ends



TYPE "ST" SPLICE

NOTES:

1. Dimensions are minimum.
2. Rubber tapes shall be rolled after application.

INSULATION METHODS

Low Voltage Circuits (0-600 V)

METHOD "B"

1. Completely cover the splice area with electrical insulating coating and allow to dry.
2. Apply 2 layers of electrical insulating pad with minimum thickness of 4 mm each layer or 2 layers, half lapped, synthetic oil resistant, self fusing rubber tape.
3. Apply 3 layers half lapped polyvinyl chloride tape.
4. Cover entire splice with electrical insulating coating and allow to dry.

High Voltage Circuits (Over 600 V)

1. Completely cover the splice area with electrical insulating coating and allow to dry.
2. Apply high voltage tape to a minimum thickness equal to original insulation.
3. Apply 3 layers half lapped polyvinyl chloride tape.
4. Cover entire splice with electrical insulating coating and allow to dry.

STATE OF CALIFORNIA
 DEPARTMENT OF TRANSPORTATION
**ELECTRICAL SYSTEMS
 (SPLICING DETAILS)**

NO SCALE
 ALL DIMENSIONS ARE IN
 MILLIMETERS UNLESS OTHERWISE SHOWN

RSP ES-13A DATED OCTOBER 5, 2007 SUPERSEDES STANDARD PLAN ES-13A
 DATED JULY 1, 2004-PAGE 478 OF THE STANDARD PLANS BOOK DATED JULY 2004.

REVISED STANDARD PLAN RSP ES-13A

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2004 REVISED STD PLAN RSP ES-13A